

Figure 1

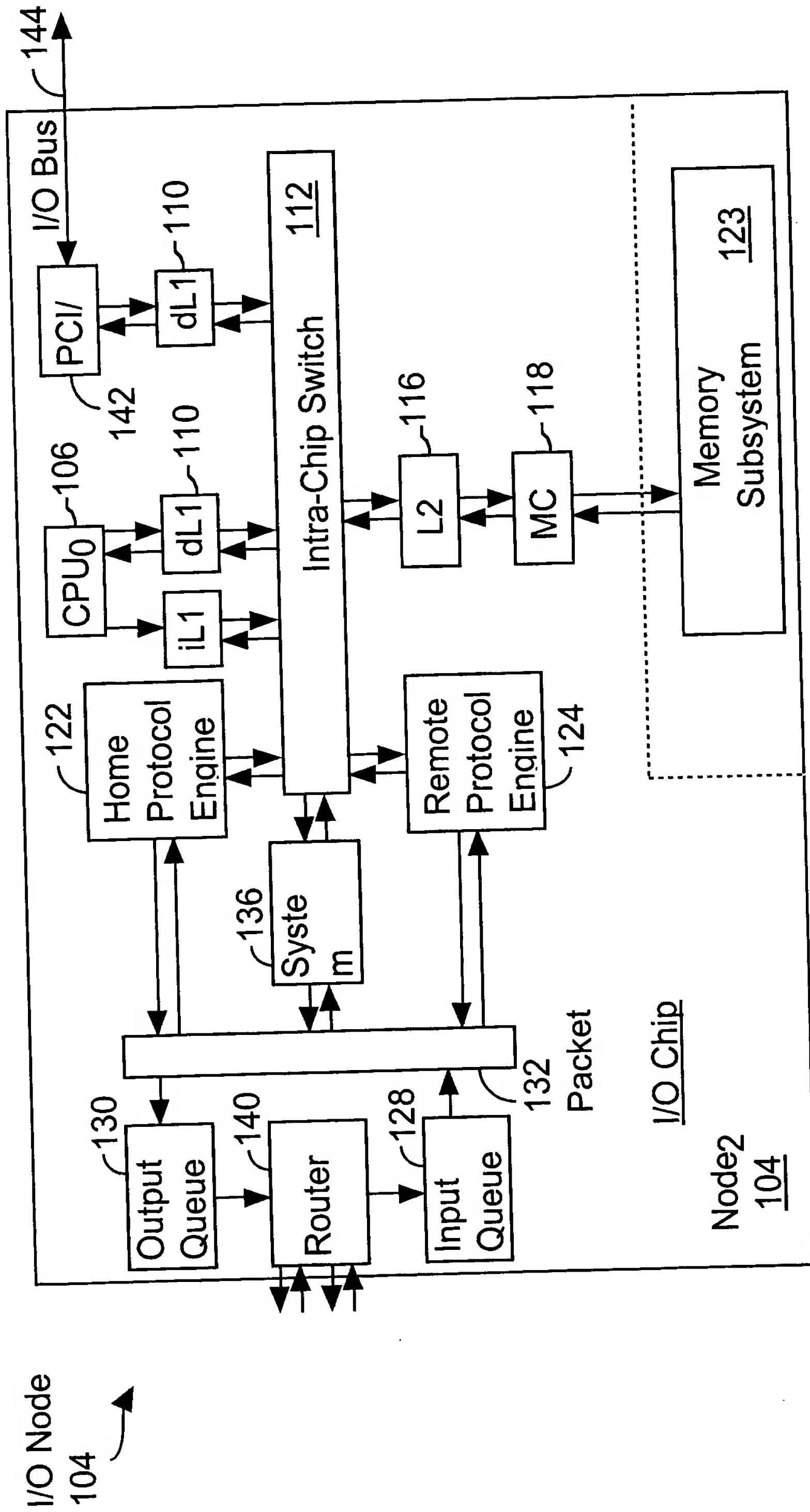
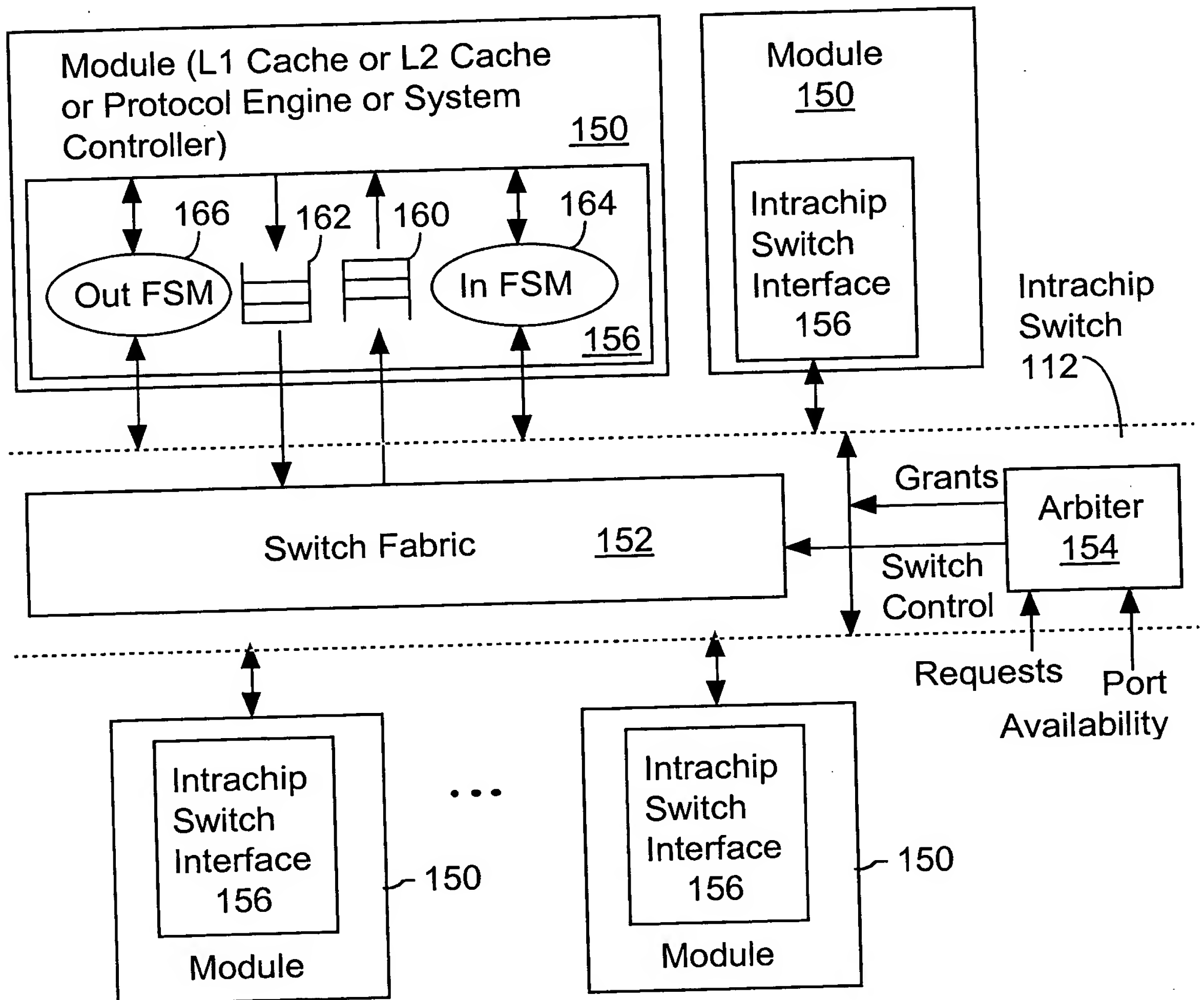
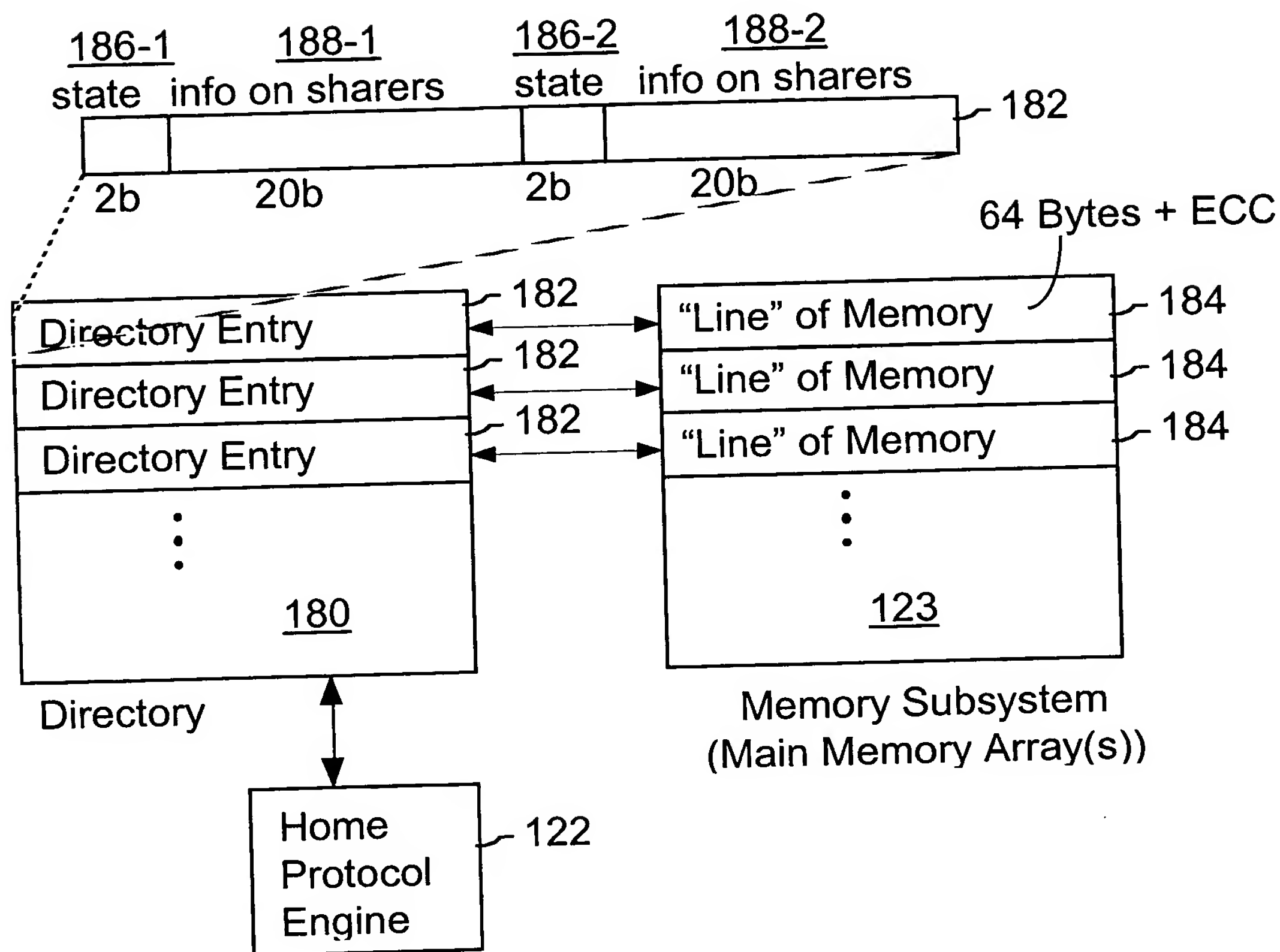


Figure 2

**Figure 3**



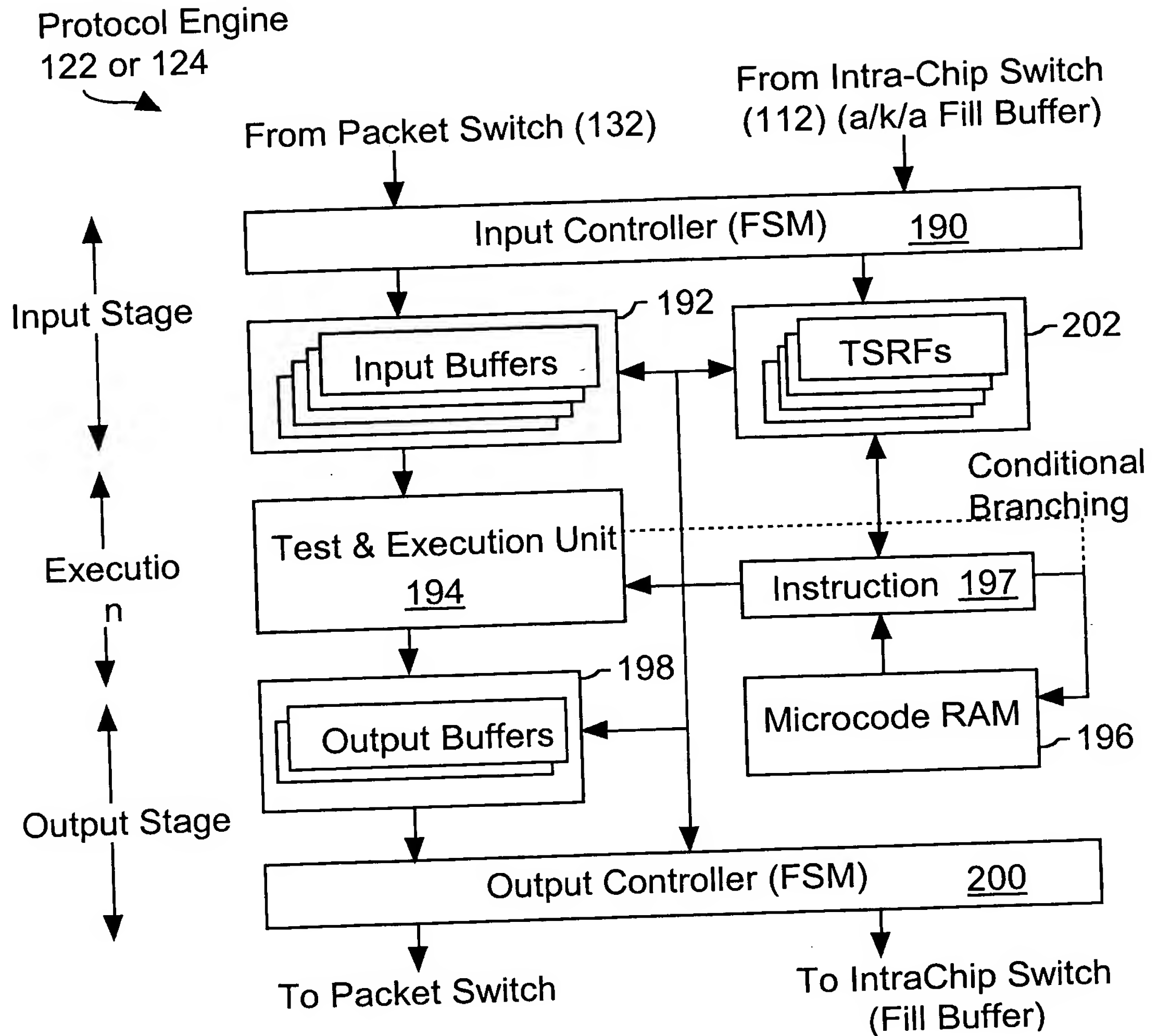
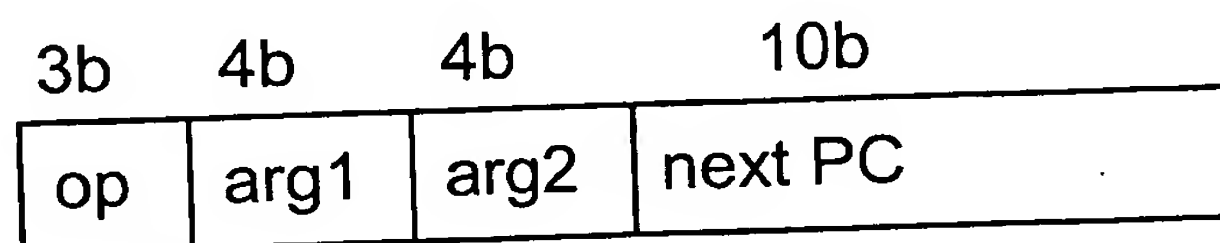
Directory State	Description
invalid	no remote copies
exclusive	exclusive remote copy
shared	one or more shared remote copies (limited pointer)
shared-cv	one or more shared remote copies (coarse pointer)

Node to Bit and Bit to Node AssignmentTable
(for sharer information field 188, coarse vector format)

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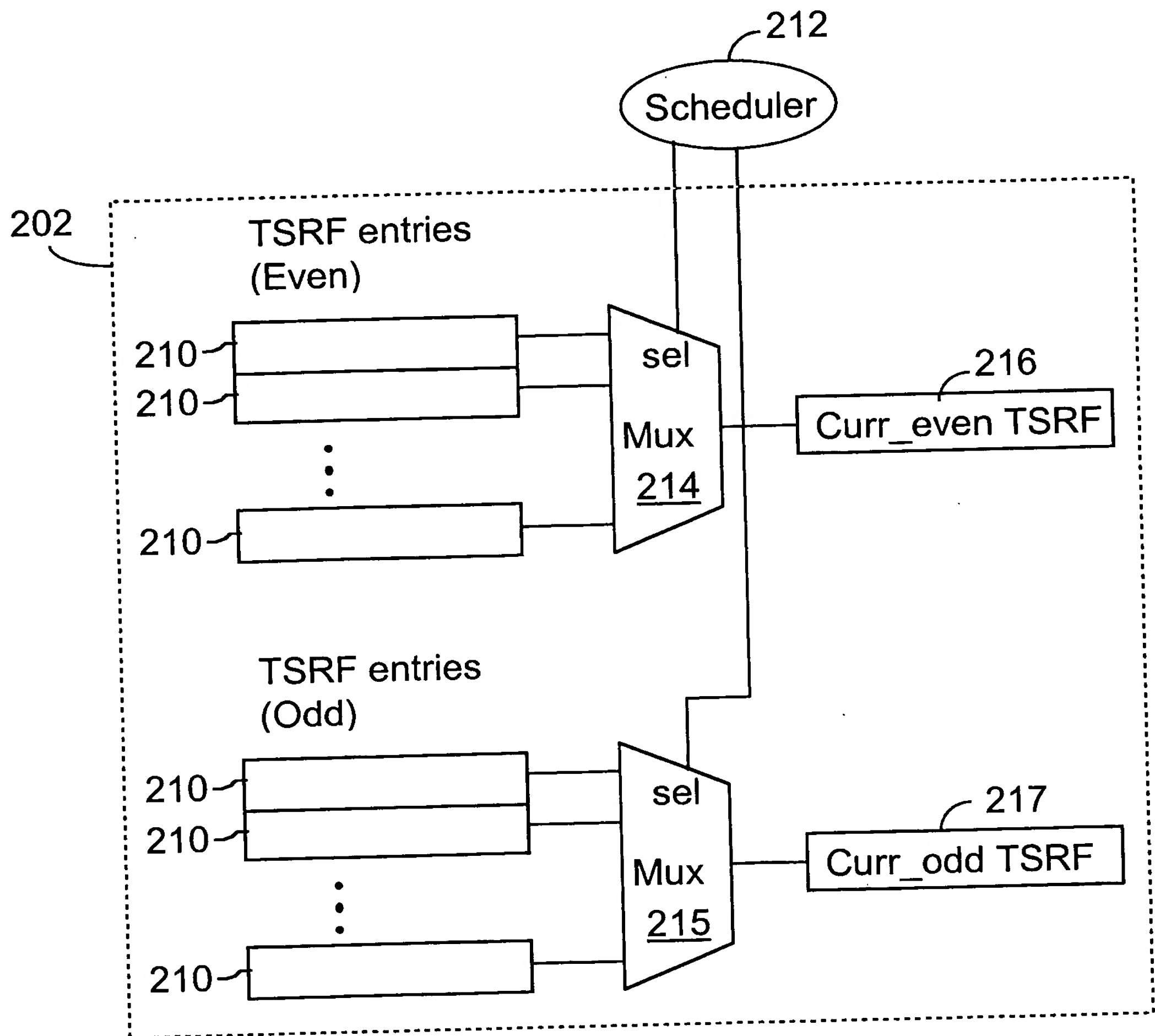
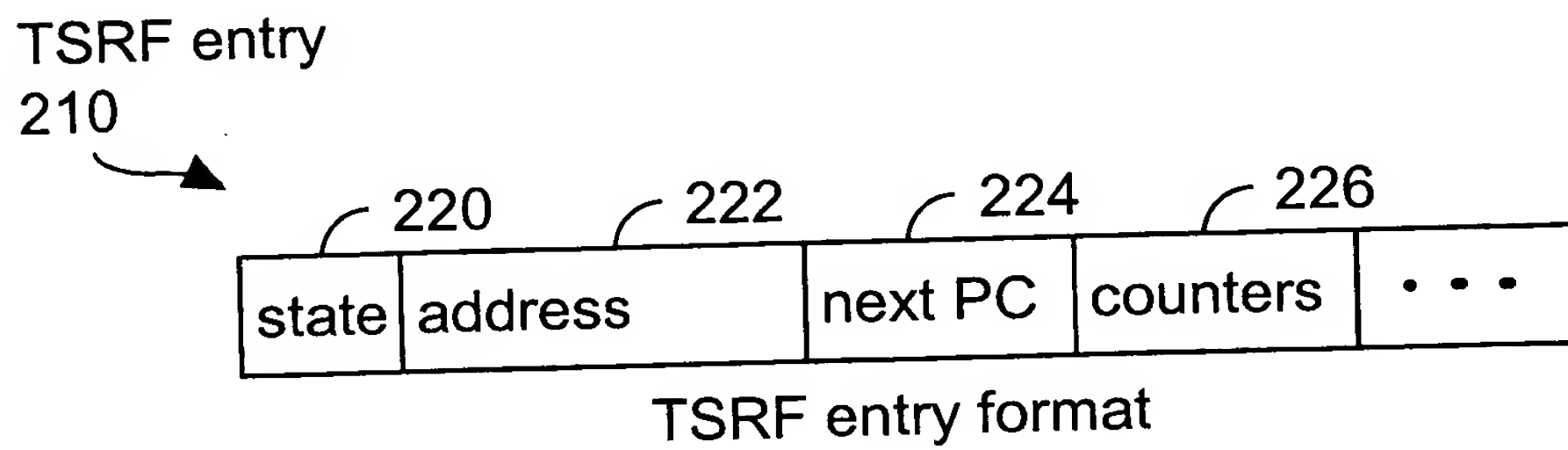
	0	1	2	3	4	5	35	36	37	38	39	
0	[0]	1	2	3	4	34	35	36	37	38	39
1	40	41	42	43	73	74	75	76			

Figure 4

**Figure 5**

Microcode Instruction Format

Figure 6A

**Figure 6B****Figure 6C**

	Even Cycle	Odd Cycle	Even Cycle	Odd Cycle
Execute	Even Tx	Odd Tx	Even Tx	Odd Tx
µCode Read	Odd Tx Instr	Even Tx Instr	Odd Tx Instr	Even Tx Instr
Schedule	Next Even	Next Odd Tx	Next Even	Next Odd Tx
TSRF Read	Odd TSRF	Even TSRF	Odd TSRF	Even TSRF

Incorporate condition codes into determination of next PC for µCode Read

Figure 7A

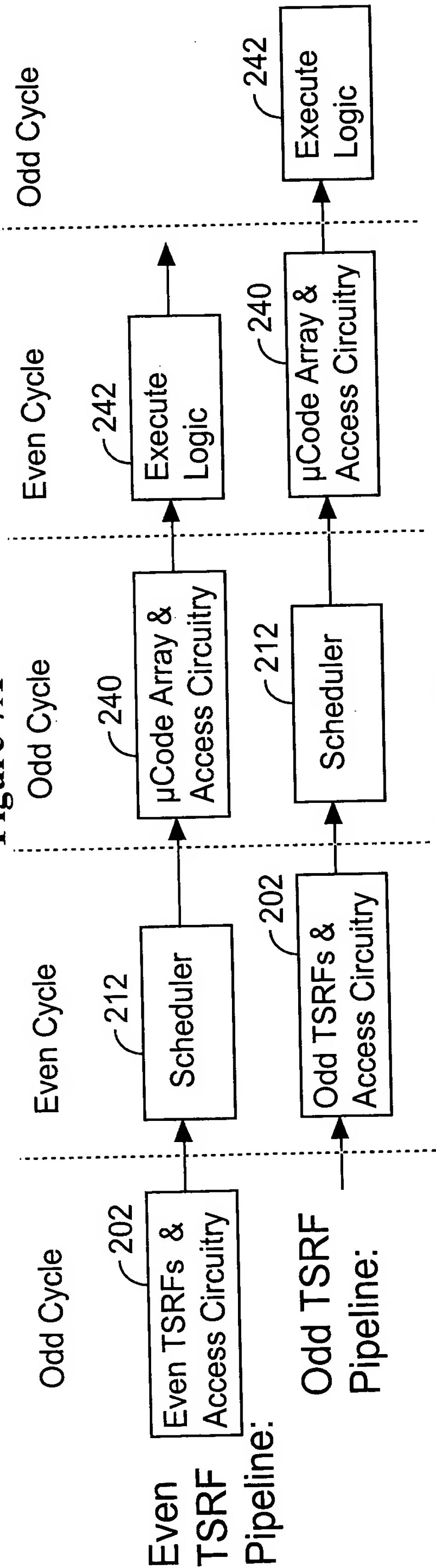


Figure 7B

TSRF State Transitions

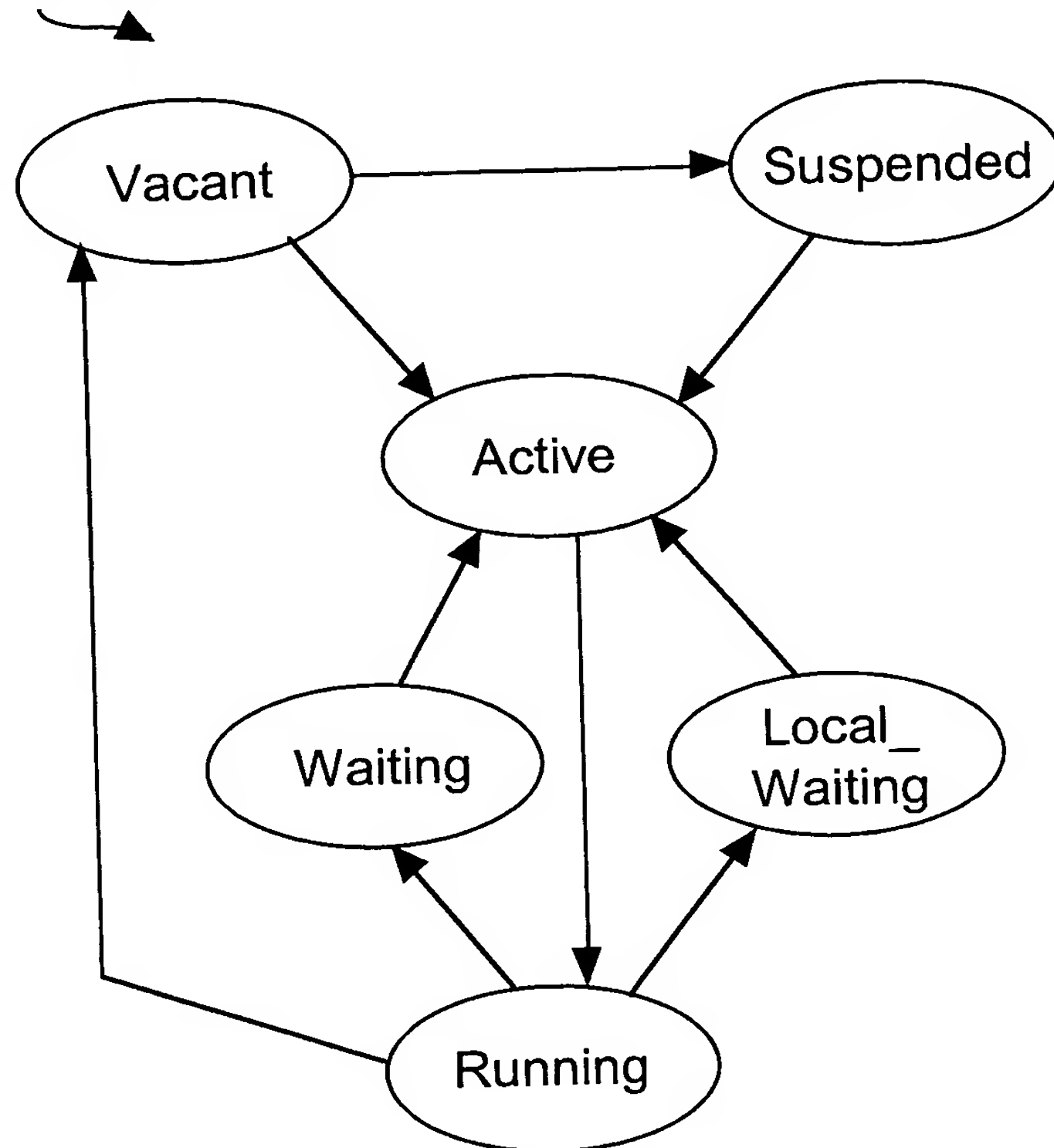


Figure 7C

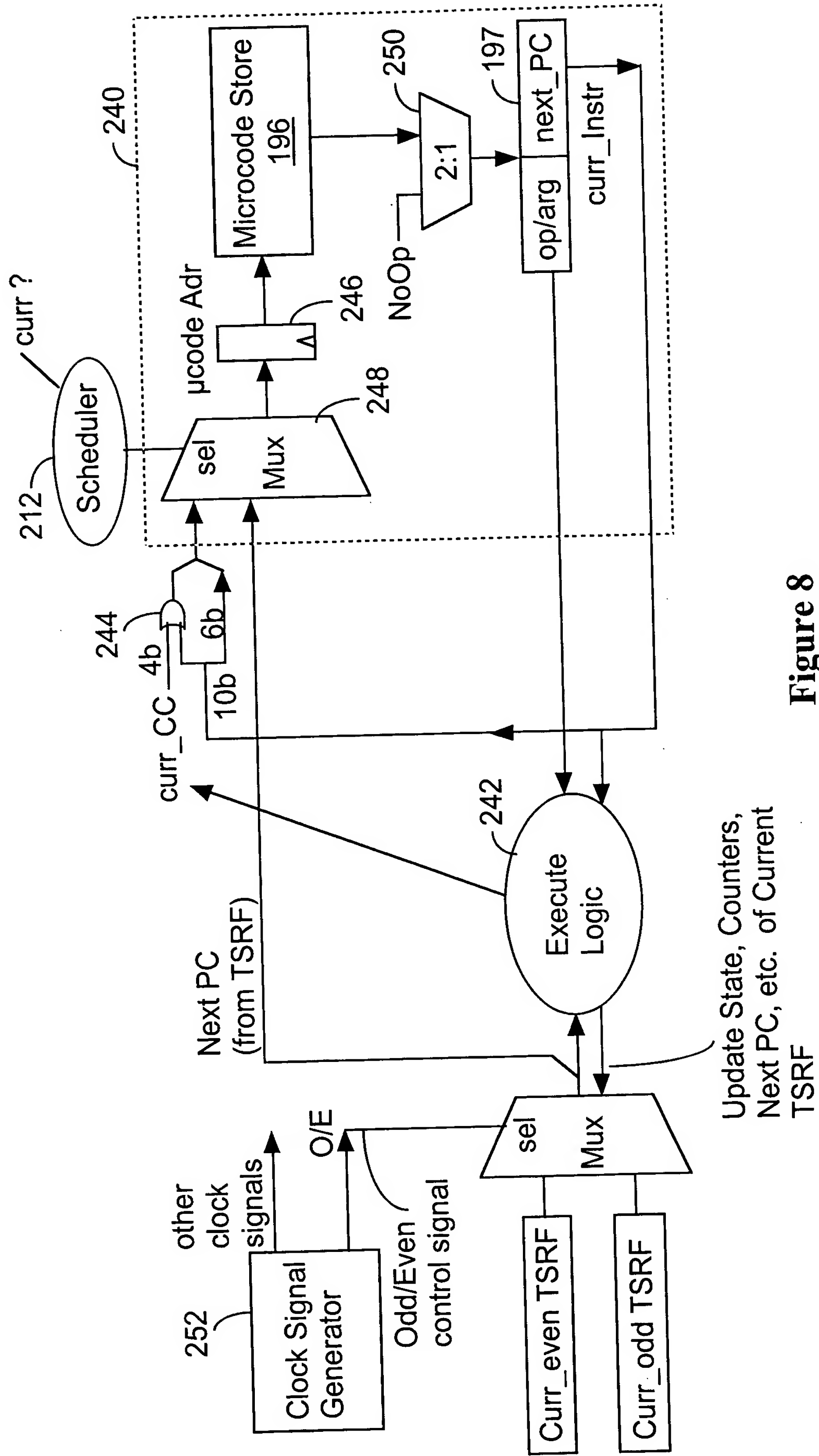
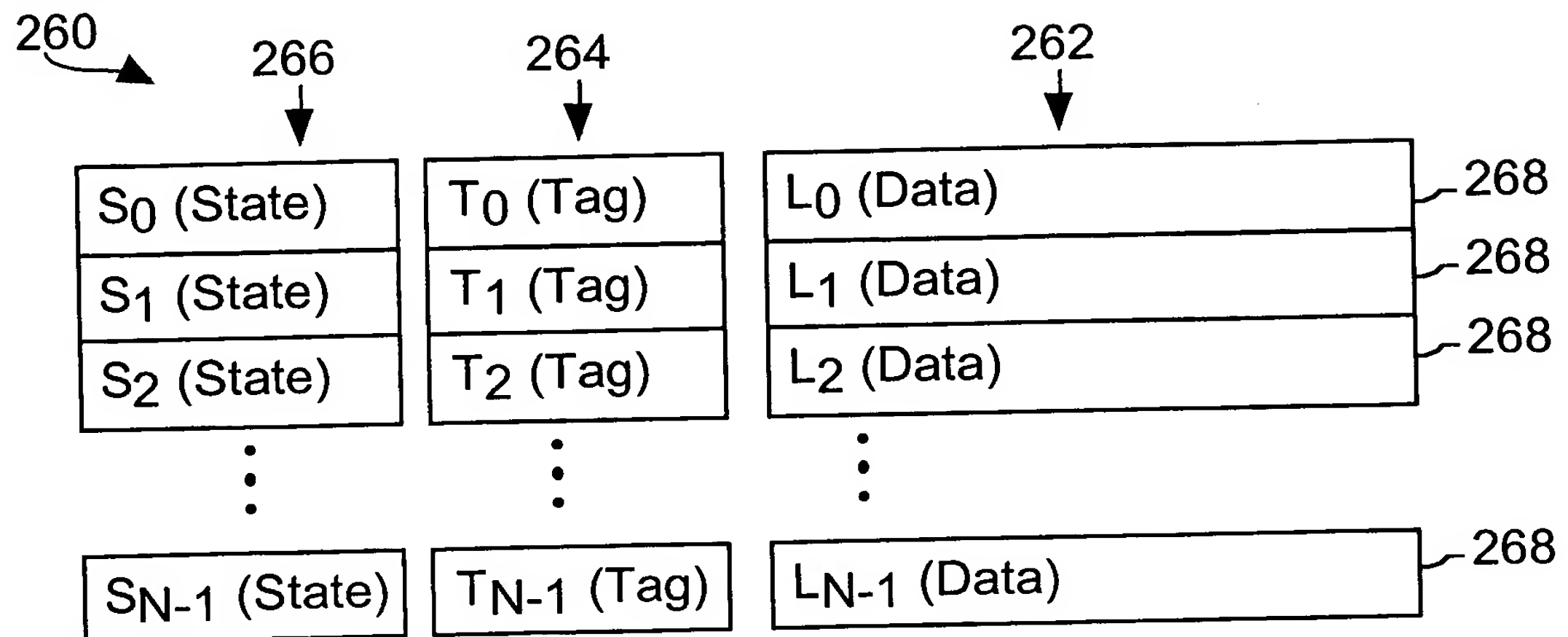


Figure 8

L1 Cache (Direct Mapped)



For Direct Mapped L1 Cache:

Address Bit Groups = ABCD

Line Address = ABC

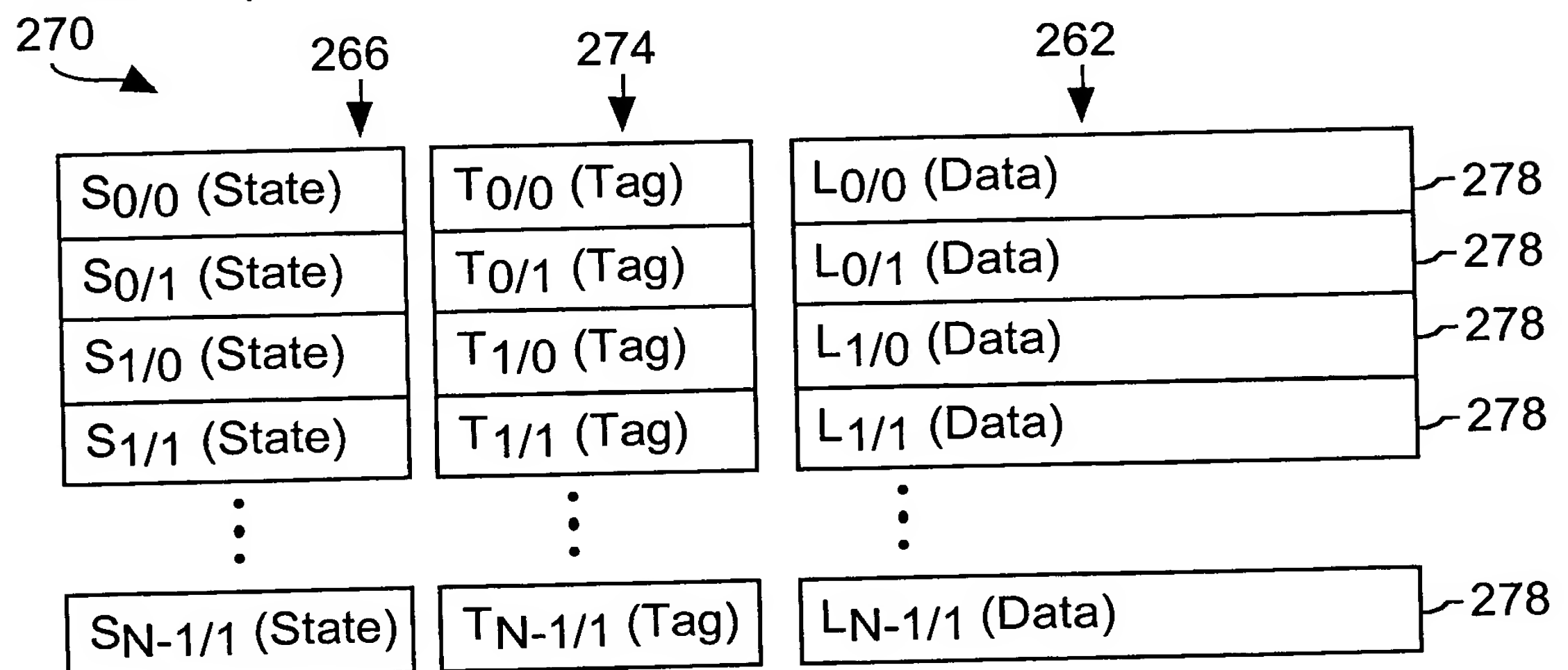
Tag = A

Cache Index for Line = BC

State = invalid, shared, clean_exclusive, dirty_exclusive

Figure 9A

L1 Cache (2 Way Set Associative)



For 2-way Set Associative Cache:

Address Bit Groups = ABCD

Line Address = ABC

Tag = AB

Cache Index for Line = C

Figure 9B

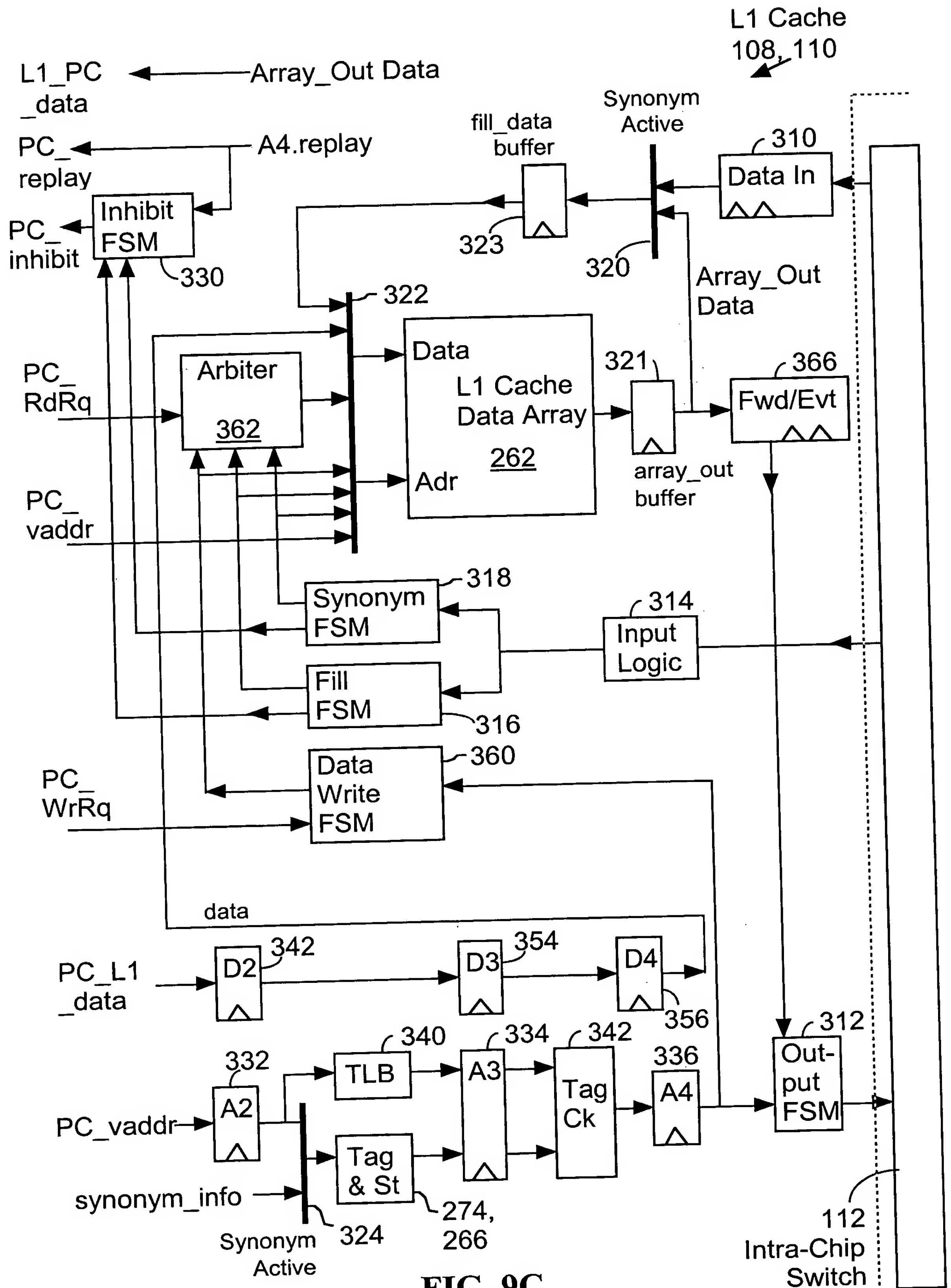


FIG. 9C

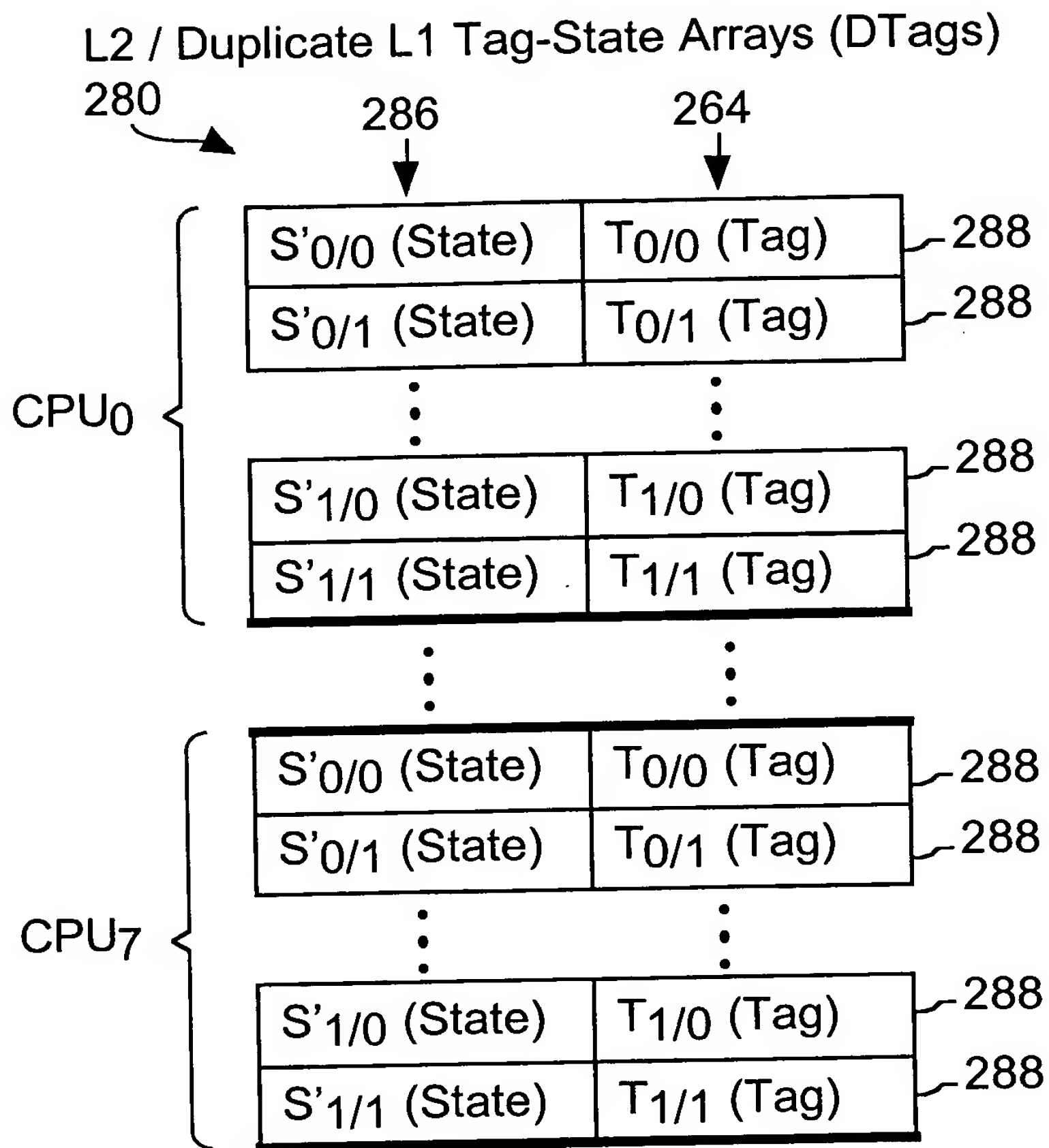


Figure 10A

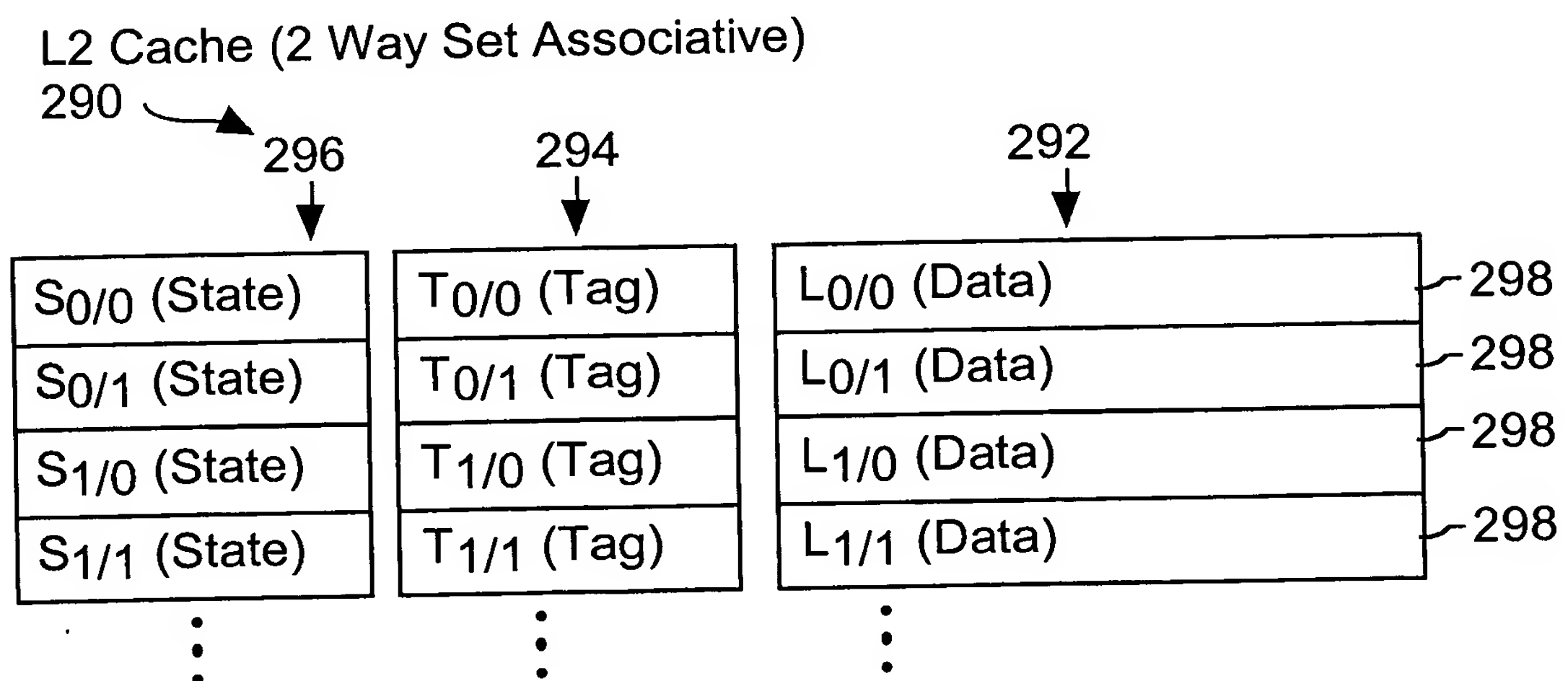


Figure 10B

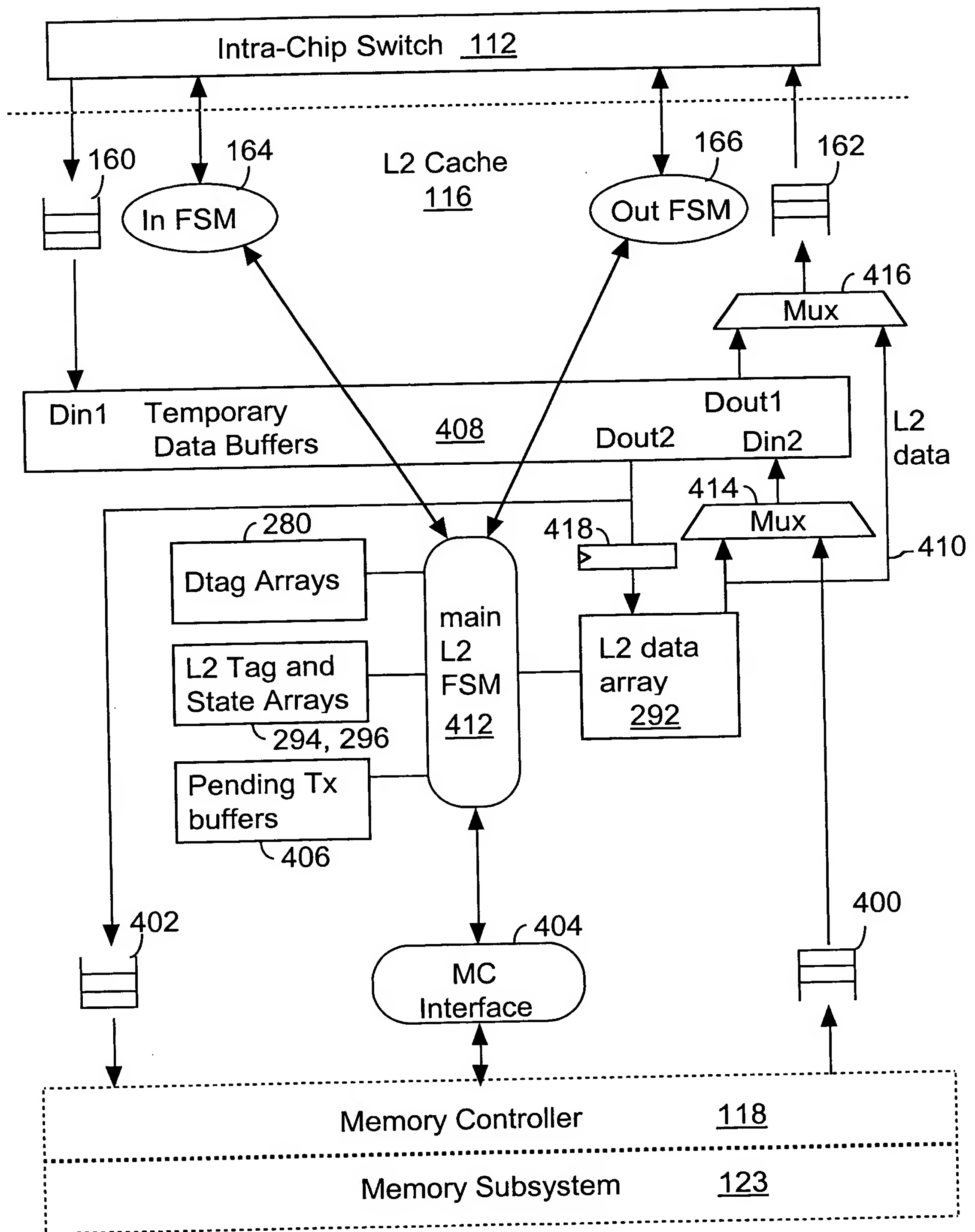


FIG. 10C

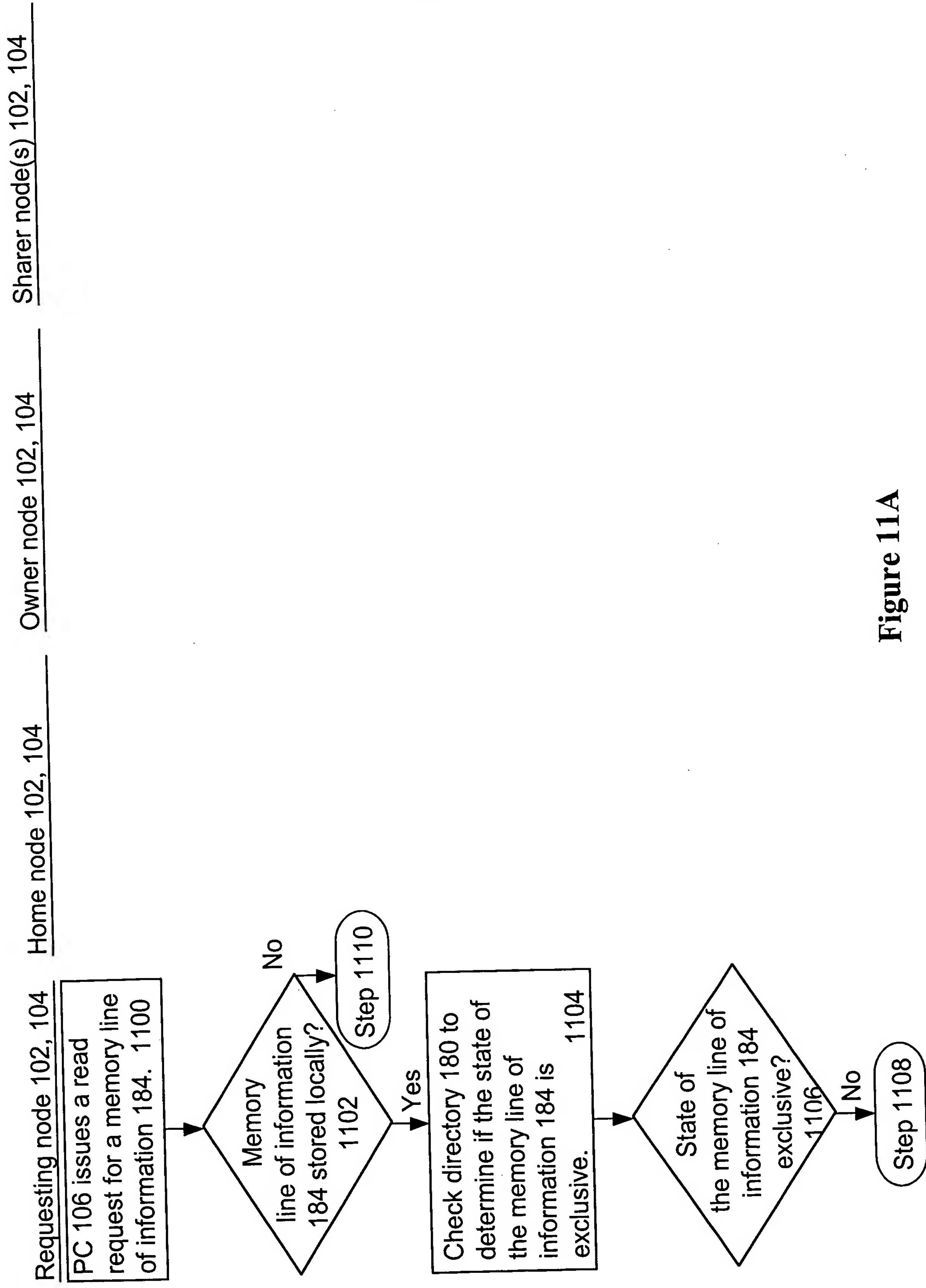


Figure 11A

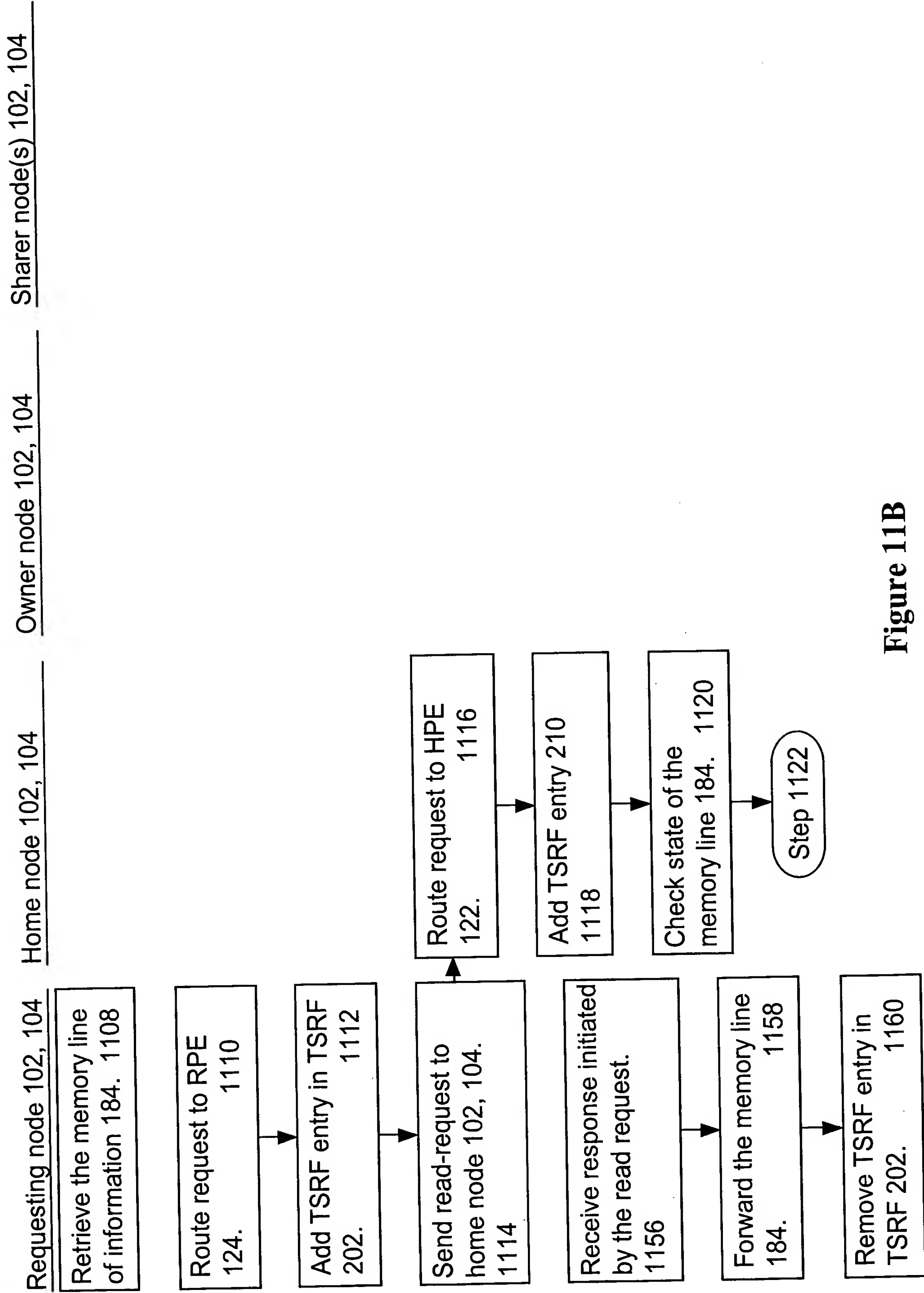


Figure 11B

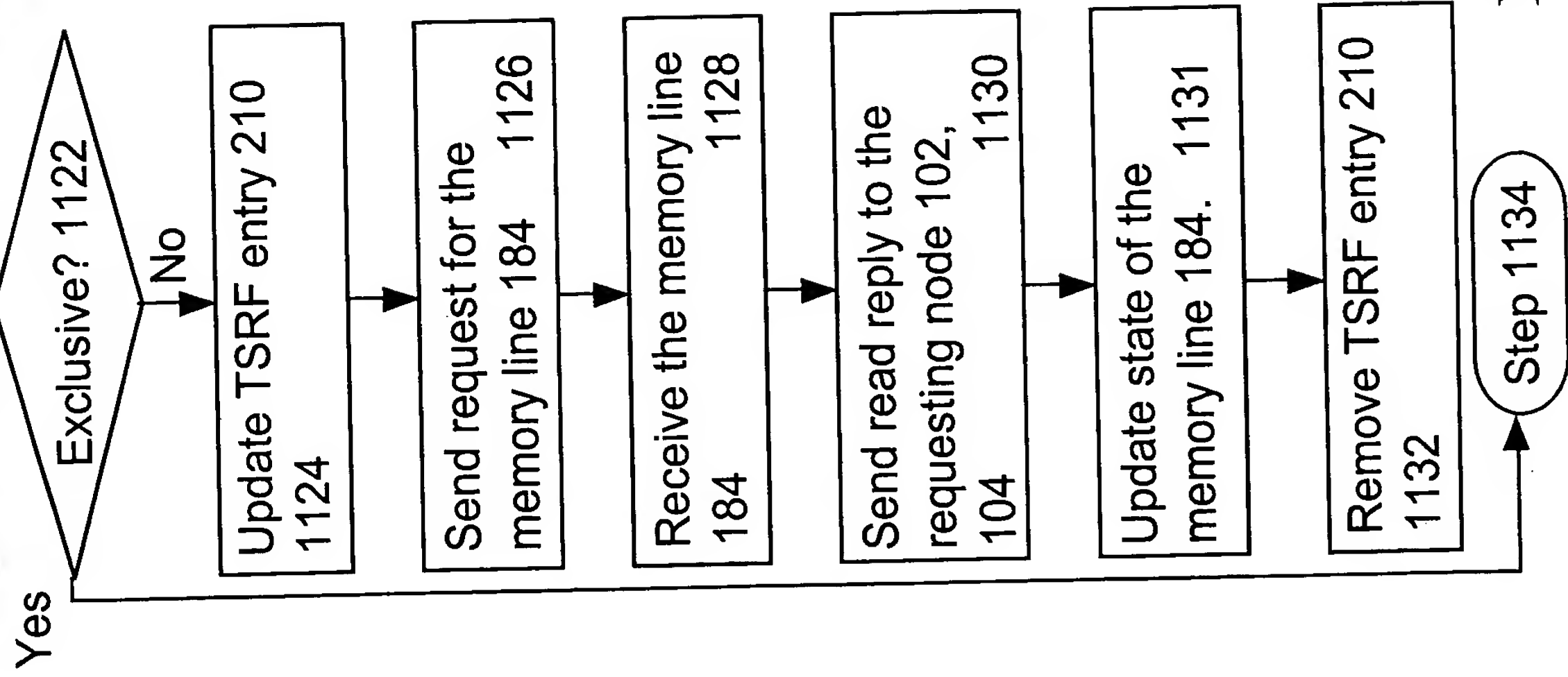


Figure 11C

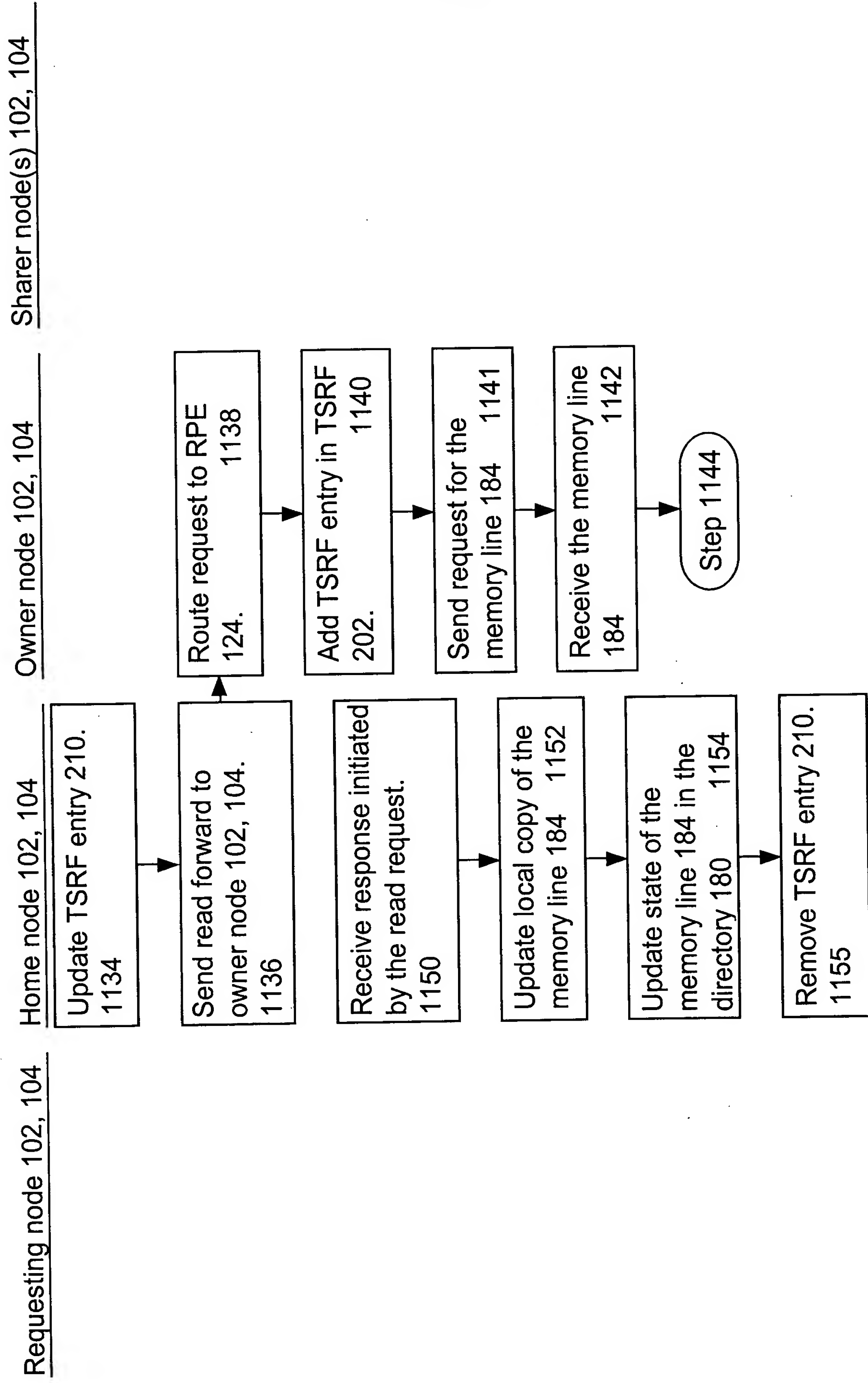


Figure 11D

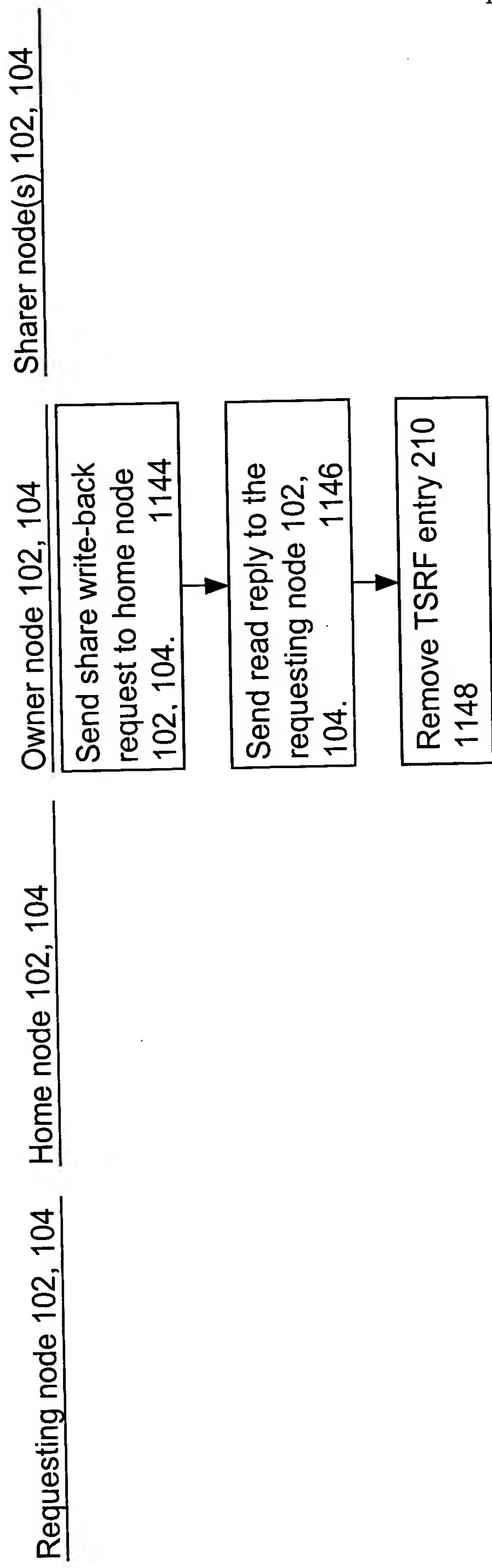


Figure 11E

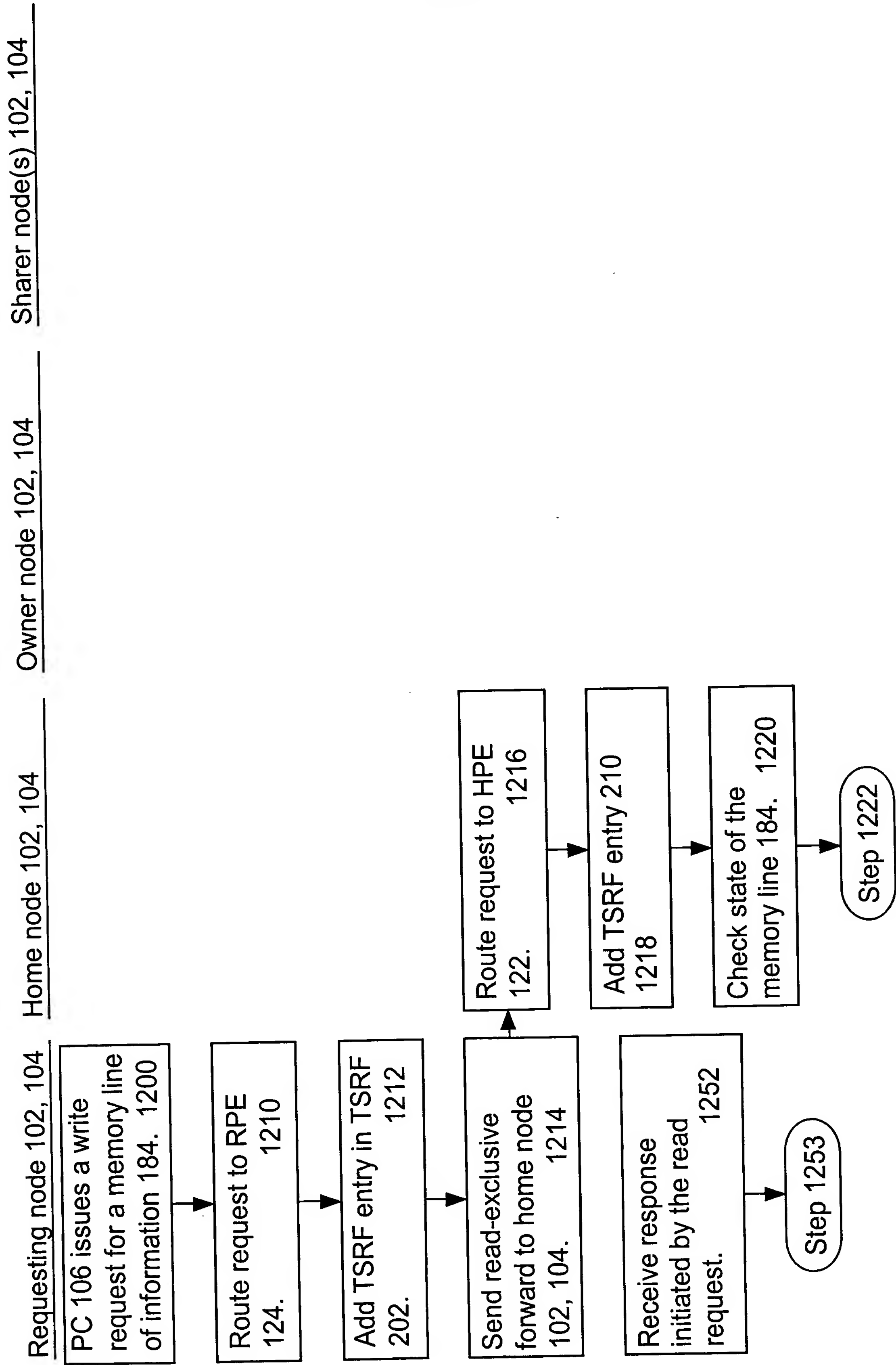


Figure 12A

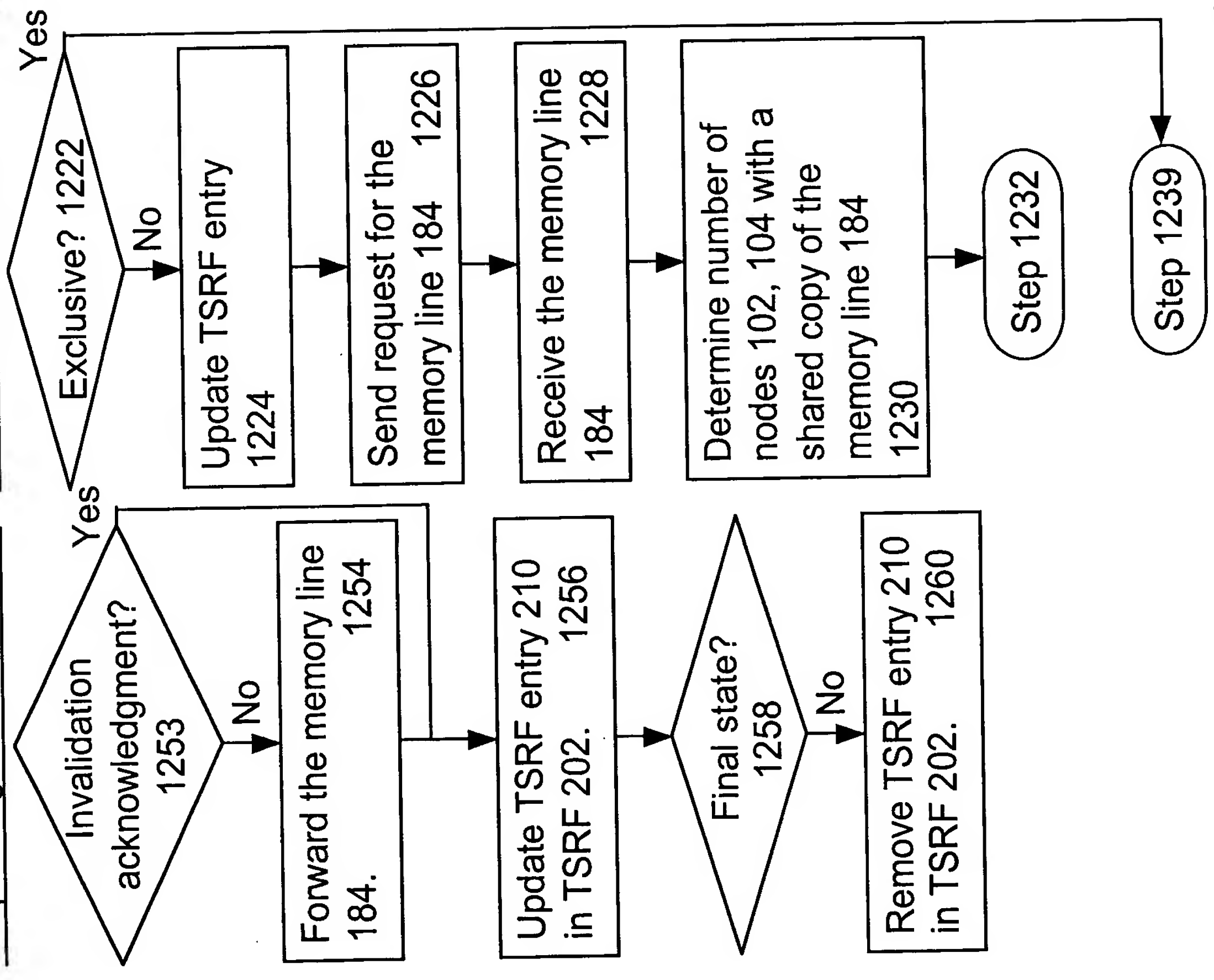


Figure 12B

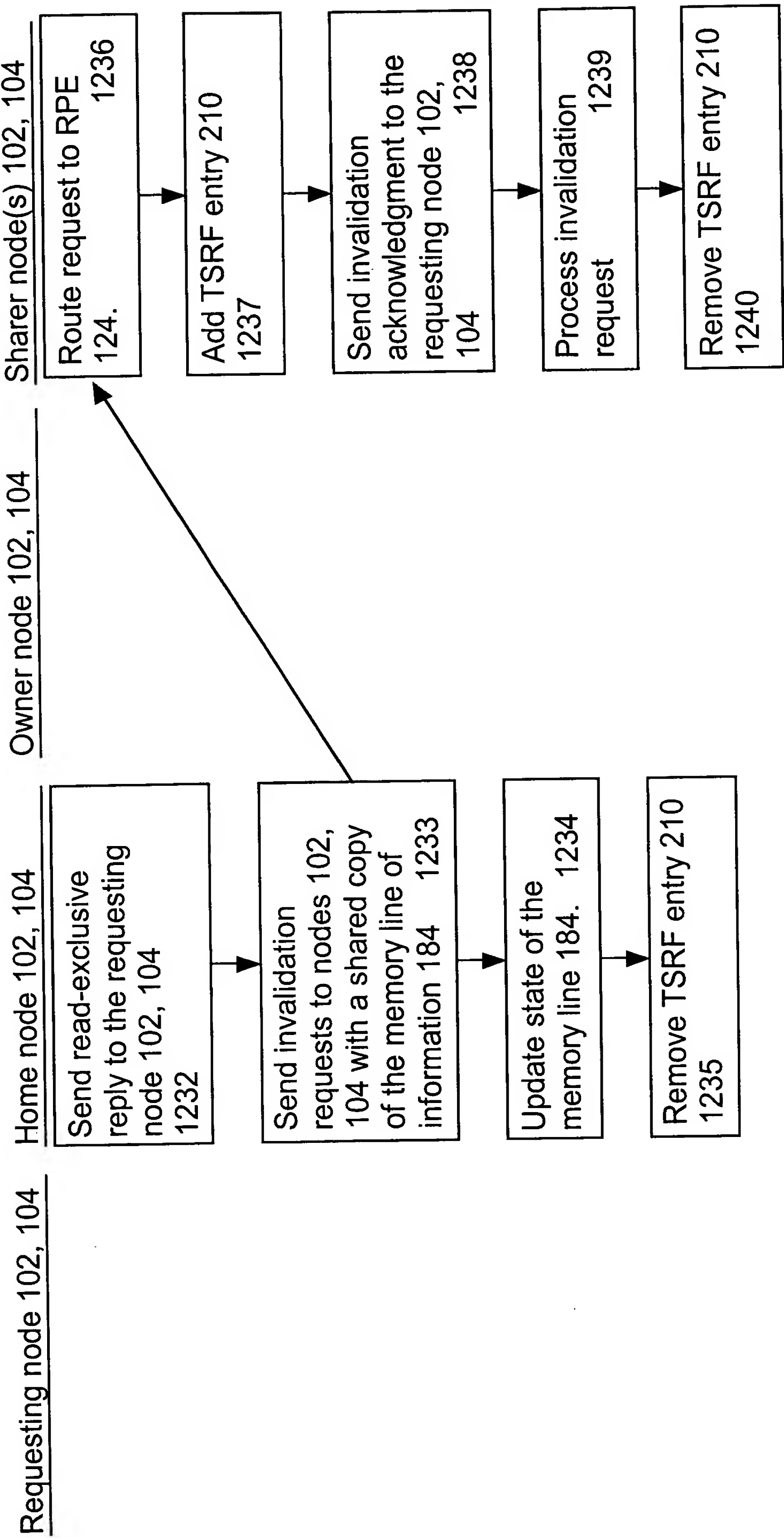


Figure 12C

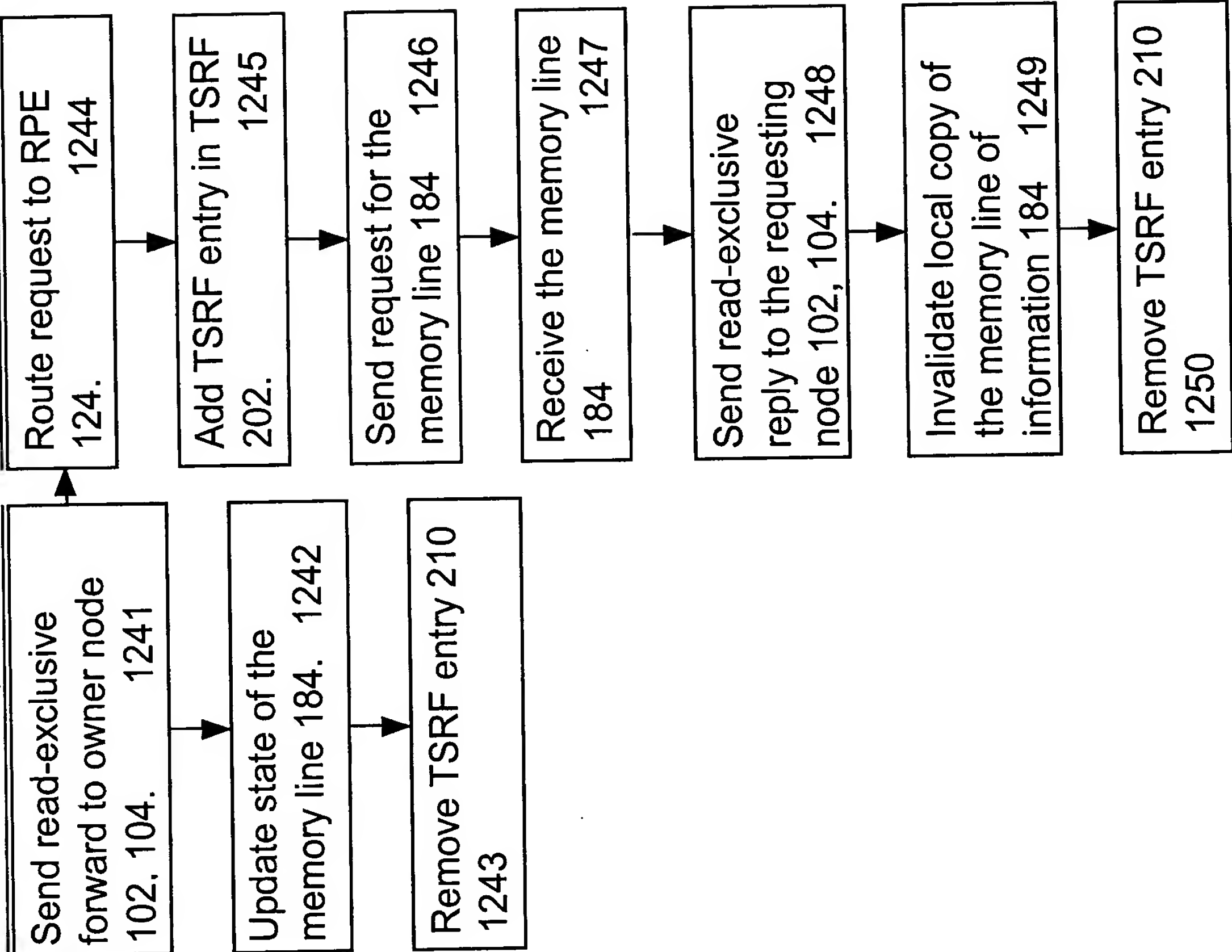


Figure 12D

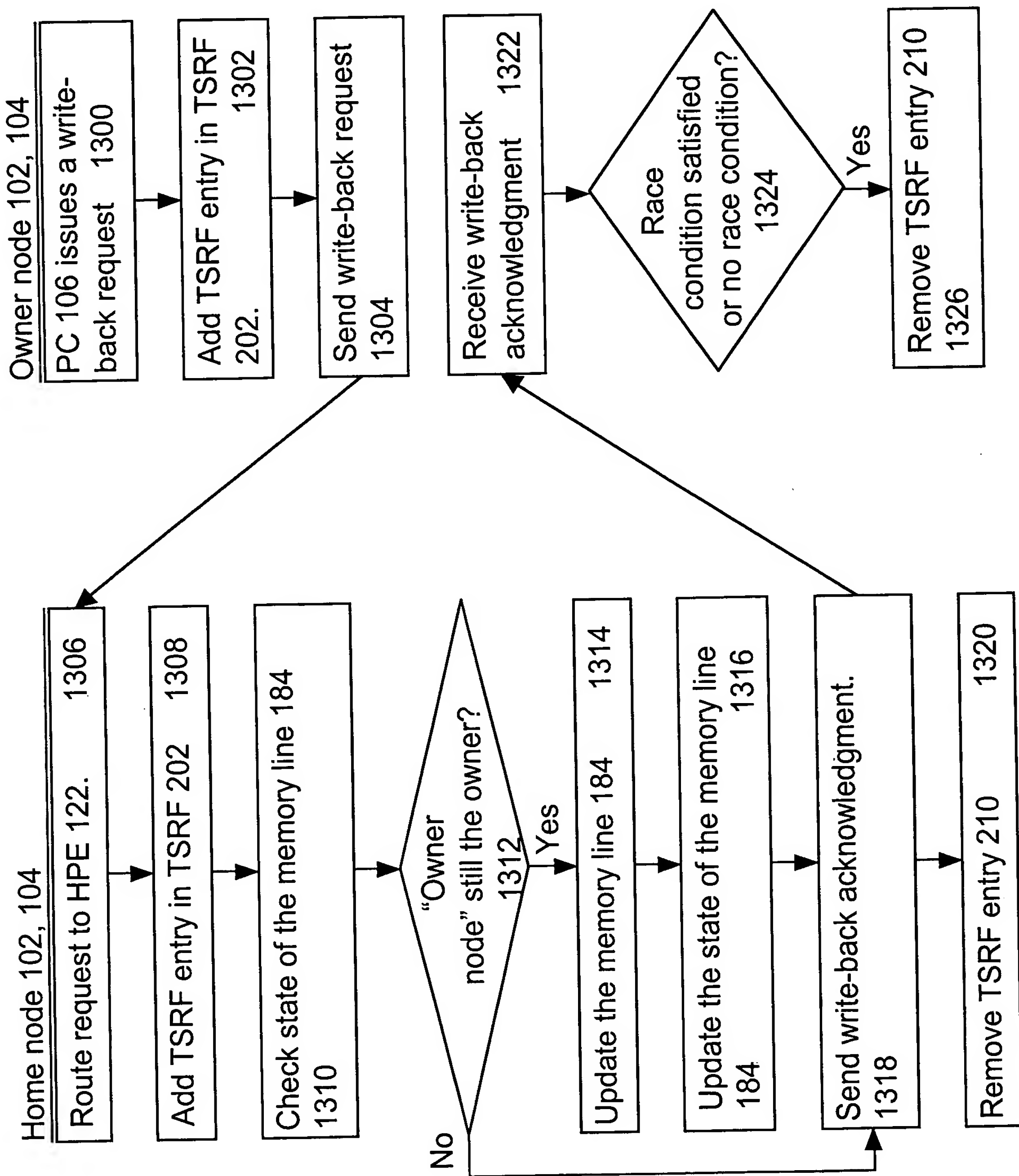


Figure 13

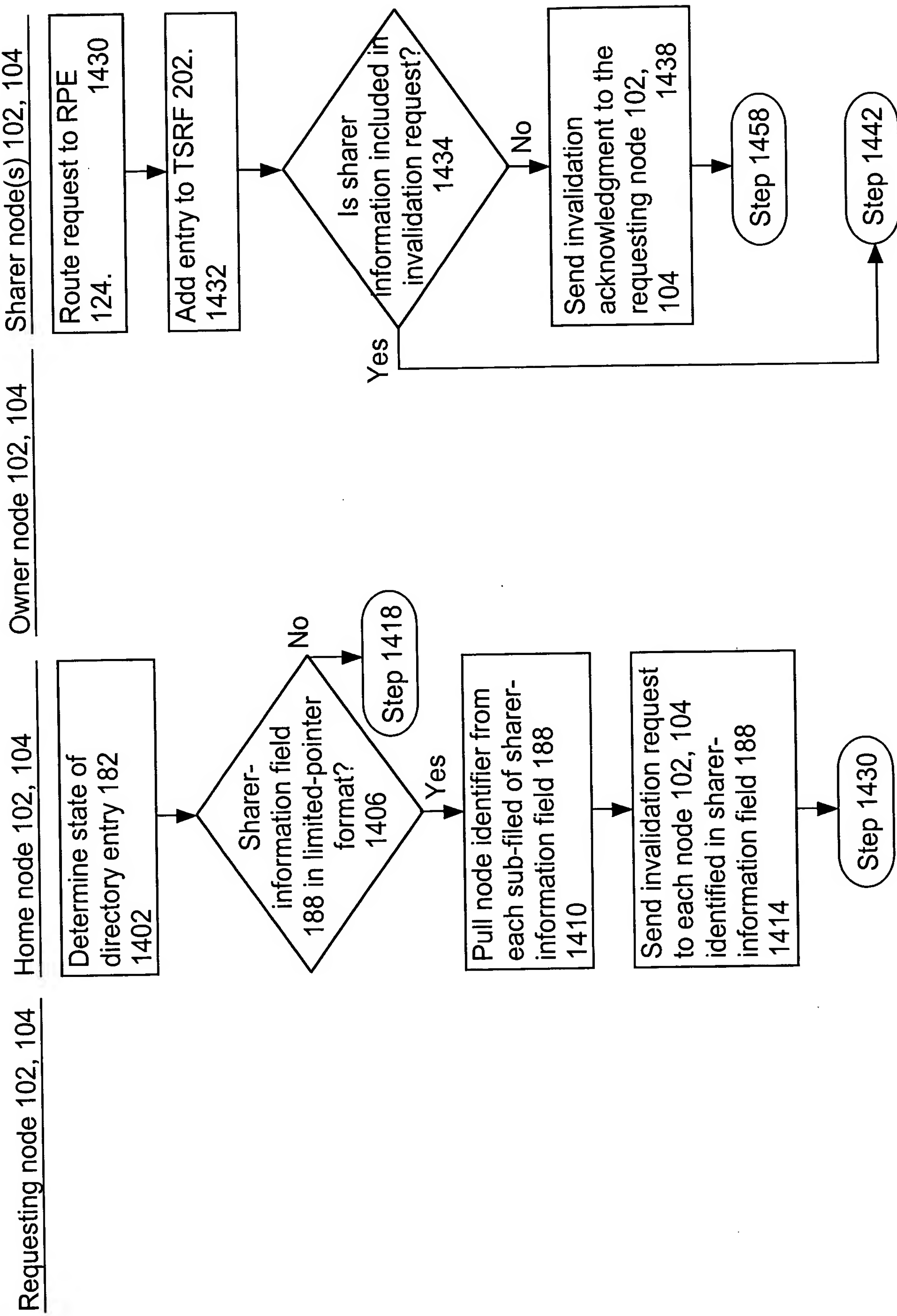


Figure 14A

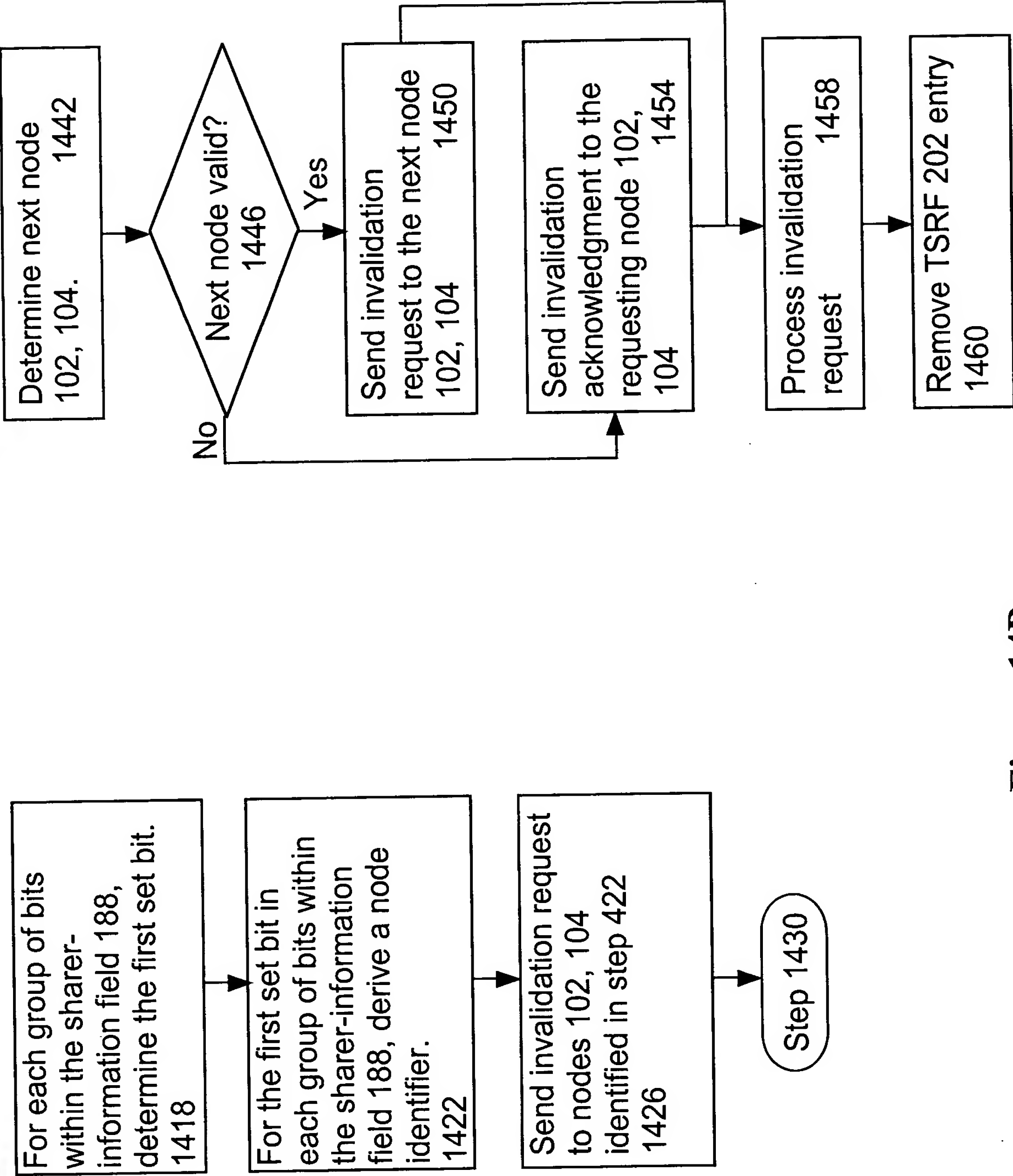


Figure 14B